BANKURA UNIVERSITY

B.Sc. 3rd Semester (Honours) Examination, March 2021

Subject: *Electronics (H)*

Course ID: 31712 Course Code: SH/ELC/302/C-6(TH)

Course Title: *Digital Electronics and Verilog*

Full Marks: 25 Time: 1Hr 15 Min

(The figures in the right hand side margin indicate marks.
Answer all the questions)

1. Answer *any three* of the following questions 1×3=3
   a) How many Half adders and Full adders will be required to add two 16 bits numbers?
   b) What is the difference between a decoder and a demultiplexer?
   c) What is sequential logic circuit? Give one example.
   d) Draw the logic circuit of one-bit comparator.
   e) Mention the name of logic gate which is used as equality detector.
   f) What are min term and max term?

2. Answer *any three* of the following questions. 2×3=6
   a) What do you mean by bipolar and unipolar logic families? Give one example of each.
   b) Convert in standard SOP form – Y = AB + AC + BC
   c) What do you mean by self-complimenting codes? Name two.
   d) What is shift register? Mention its two applications.
   e) What is sign-magnitude representation? Represent $(-15)_{10}$ in this representation.
   f) What is 'Propagation delay time' and 'fan out' of a logic gate?

3. Answer *any two* of the following questions. 5×2=10

a) Draw the logic symbol of clocked R-S flip-flop and give its truth table. How will you get D and T flip-flop from JK flip-flop?

b) What is full subtractor? Write down its truth table. Implement a full subtractor using demultiplexer.

c) Explain CMOS inverter with proper circuit diagram. Compare CMOS and TTL families.

d) Perform the following:

(i) $(-5)_{10}$+¿ using 1's complement method.

(ii) $(15)_{10} - (21)_{10}$ using 2's complement method.

4. Answer *any one* of the following questions. 6×1=6

a) Implement the following Boolean expression using multiplexer:

$$Y = (A + B) (A + B + C) (A + B)$$

b) Design MOD -10 counter using JK flip-flop and explain its operation in brief. Draw its timing diagram.

c) Explain the working of a Half subtractor with logic diagram and truth table. Realize it using NOR gates only.